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Topic:

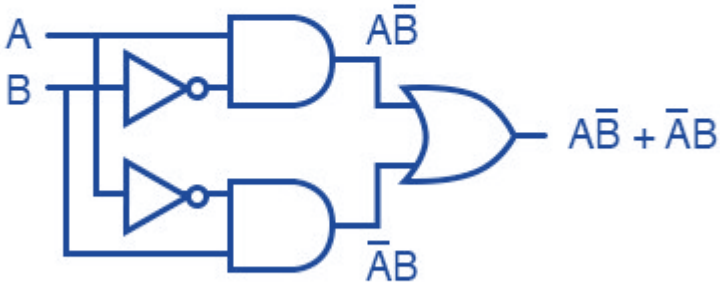
Digital Circuits: X-OR & X-NOR Gates, 2's compliment, Subtraction by 2's compliment, Half Adder, Full Adder

Digital Circuits:

X-OR & X-NOR Gates:

XOR Gate (**Exclusive OR**) is a digital logic **Gate** that gives a true (1 or HIGH) output when the number of inputs is only odd.

. . . is equivalent to . .



$A \oplus B = A\bar{B} + \bar{A}B$

Truth Table:

A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

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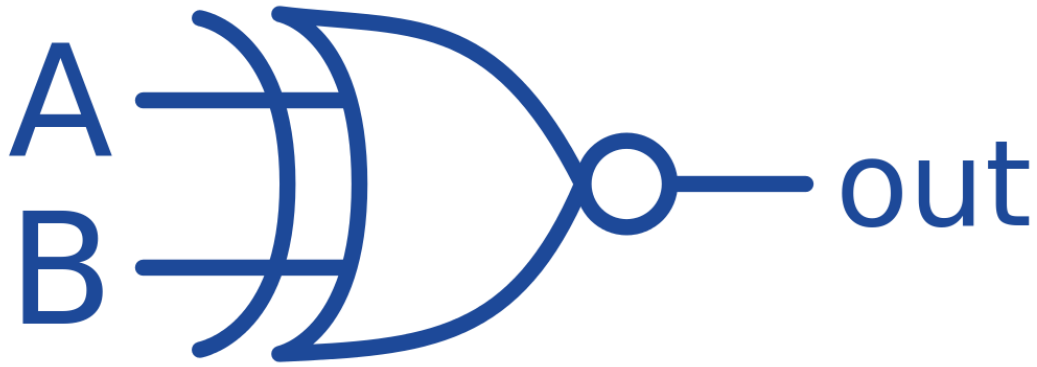
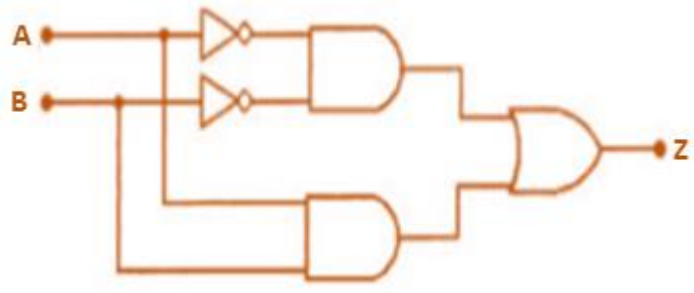
X-NOR Gates:

The XNOR gate (Exclusive NOR) is a digital logic gate whose function is the logical complement of the Exclusive OR (XOR) gate.



Symbol of X-NOR Gate



Construction of X-NOR Gate: $\boldsymbol{Y = AB + \overline{AB}}$

Truth Table:

A	B	X-NOR $Y = AB + \overline{AB}$
0	0	1
0	1	0
1	0	0
1	1	1

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1's and 2's complement:

1's complement of a binary number is another binary number obtained by transforming the 0 bit to 1 and the 1 bit to 0.

Examples:

1's complement of (0111) is (1000)

1's complement of (1100) is (0011)

2's complement of a binary number is 1 added to the 1's complement of the binary number.

Examples:

2's complement of (0111) is (1000 + 1=1001)

In subtraction by 1's complement we subtract two binary numbers using carried by 1's complement.

Subtraction by 1's complement :

Evaluate:

(i) 110101 – 100101

1's complement of 100101 is 011010. Hence

Minued - 1 1 0 1 0 1

1's complement of subtrahend - + 0 1 1 0 1 0

Carry over - 1 0 0 1 1 1 1

+ 1

0 1 0 0 0 0

The required difference is 10000 (Ans)

(ii) 101011 – 111001

Solution:

1's complement of 111001 is 000110. Hence

Minued - 1 0 1 0 1 1

1's complement - +0 0 0 1 1 0

1 1 0 0 0 1 **(No carry)**

Hence the difference is – 1 1 1 0 (Ans)

Subtraction using 2's Complement

These are the following steps to subtract two binary numbers using 2's complement

- In the first step, we have to find the 2's complement of the subtrahend.
- Then, we have to add the complement number with the minuend.
- After adding, if we get the carry by adding both the numbers, then we discard this carry and the result is positive else take 2's complement of the result which will be negative.

Example 1: Substract: 10101 - 00111

We take 2's complement of subtrahend 00111, which is 11001. Now, sum them. So,

10101+11001 =**1** 01110

In the above result, we get the carry bit 1. So we discard this carry bit and remaining is the final result and a positive number.

Hence the difference is 0 1 1 1 0 (Ans)

Example 2: Substract: 10101 - 10111

We take 2's complement of subtrahend 10111, which comes out 01001. Now, we add both of the numbers. Hence,

10101+01001 =11110

In the above result, we didn't get the carry bit. So calculate the 2's complement of the result, i.e., 00010. It is the negative number and the final answer.

Hence the difference is 0 0 0 1 0 (Ans)

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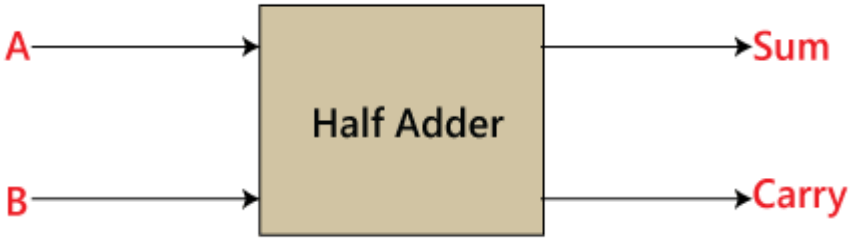
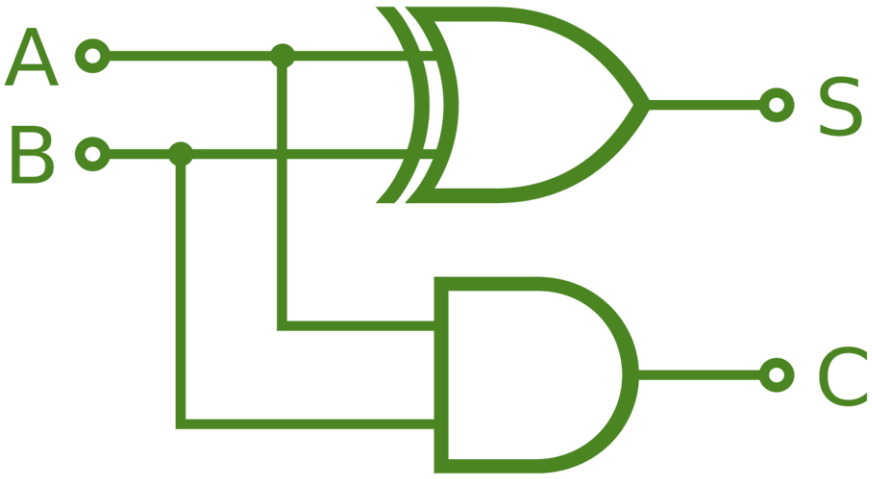
Half Adder

Half Adder is combinational logic circuit which sums two 1-bit digits. The half adder produces a sum of the two inputs. A half adder is used for adding together the two least significant digits in a binary sum. The half adder can add only two input bits (A and B) and has nothing to do with the carry if there is any in the input. That means the binary addition process is not complete and that's why it is called a half adder.



Symbol/Block Diagram of Half Adder



Circuit Diagram of Half Adder

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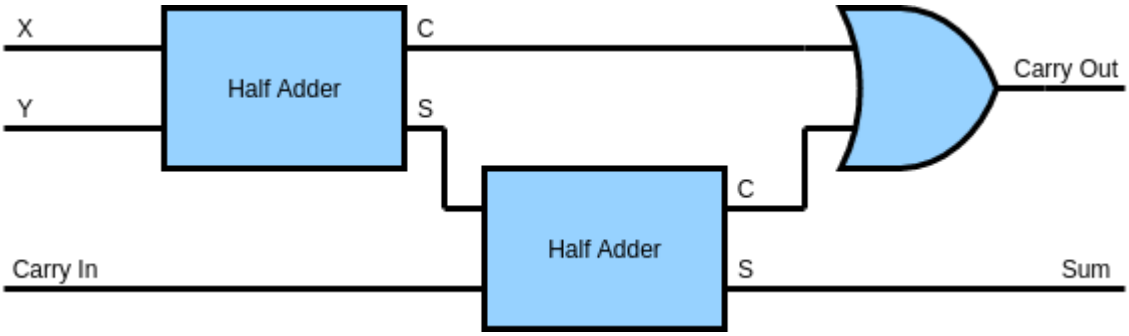
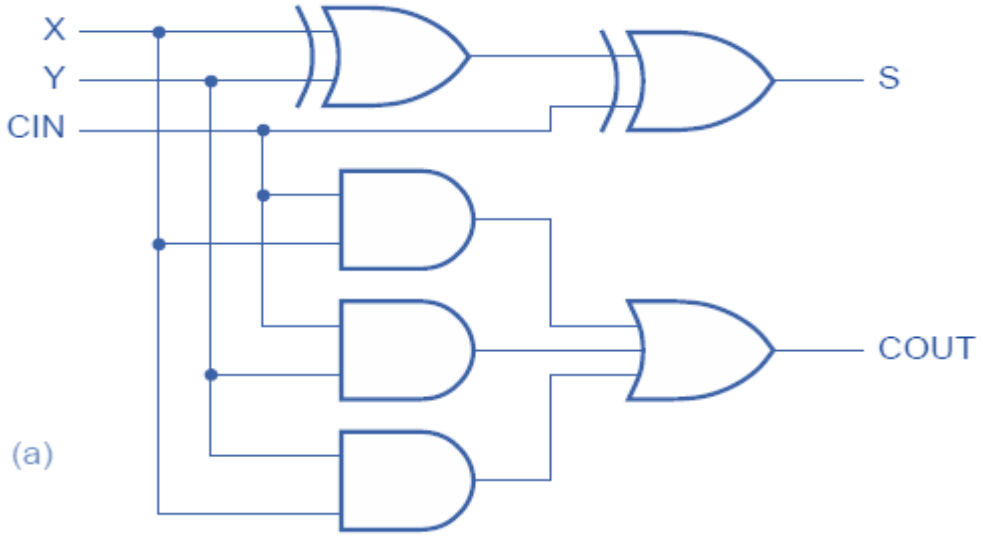
Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table of Half Adder

Full Adder



Symbol/Block Diagram of Full Adder



Circuit Diagram of Full Adder

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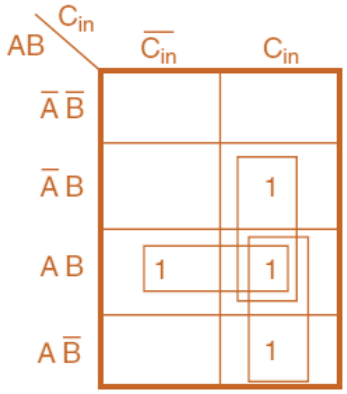
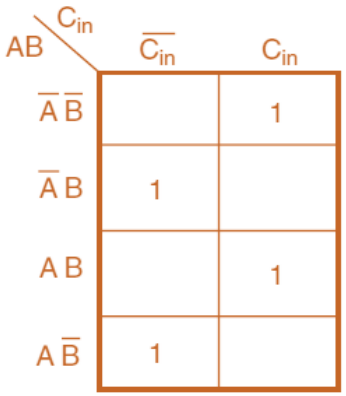
Input			Output	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table of Full Adder

A	B	C_{in}	SUM (S)	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1





$C_{out} = \overline{A}.B.C_{in} + A.\overline{B}.C_{in} + A.B.\overline{C}_{in} + A.B.C_{in}$

$S = \overline{A}.\overline{B}.C_{in} + \overline{A}.B.\overline{C}_{in} + A.\overline{B}.\overline{C}_{in} + A.B.C_{in}$

K-Map for Full Adder

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$$\text{Sum} = \bar{A}\,\bar{B}\,C_{in} + \bar{A}\,B\,\bar{C}_{in} + A\,\bar{B}\,\bar{C}_{in} + A\,B\,C_{in}$$

$$= C_{in}\left(\bar{A}\,\bar{B} + A\,B\right) + \bar{C}_{in}\left(\bar{A}\,B + A\,\bar{B}\right)$$

$$= C_{in}\left(A \odot B\right) + \bar{C}_{in}\left(A \oplus B\right)$$

$$= C_{in}\left(\overline{A \oplus B}\right) + \bar{C}_{in}\left(A \oplus B\right)$$

$$= C_{in} \oplus \left(A \oplus B\right)$$

$$\text{Carry} = AB + AC_{in} + BC_{in}$$

$$= AB + AC_{in}\left(B + \bar{B}\right) + BC_{in}\left(A + \bar{A}\right)$$

$$= AB + ABC_{in} + A\bar{B}C_{in} + ABC_{in} + \bar{A}BC_{in}$$

$$= AB\left(1 + C_{in} + C_{in}\right) + A\bar{B}C_{in} + \bar{A}BC_{in}$$

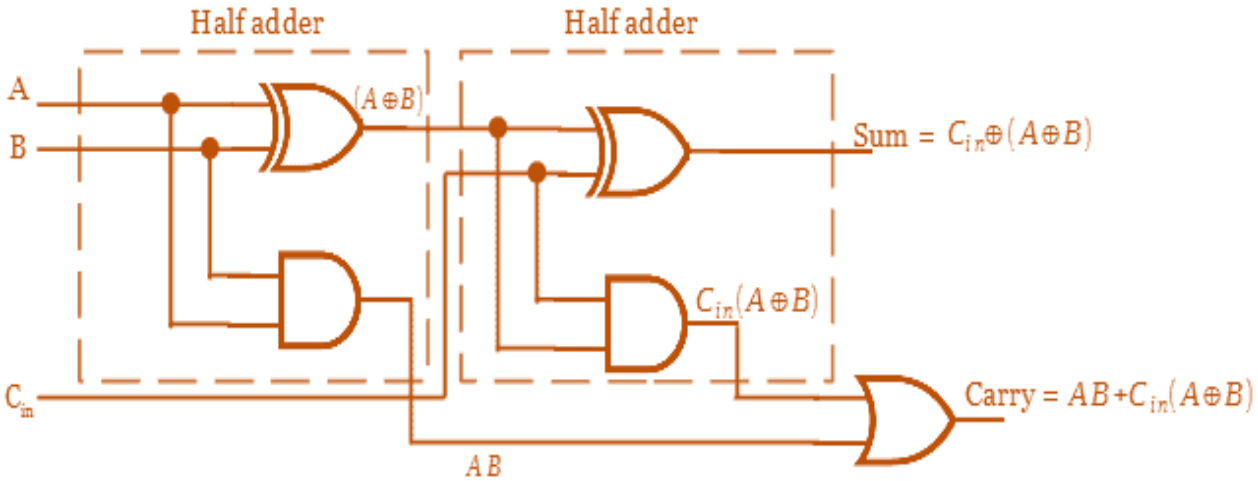
$$= AB + A\bar{B}C_{in} + \bar{A}BC_{in}$$

$$= AB + C_{in}\left(A\bar{B} + \bar{A}B\right)$$

$$= AB + C_{in}\left(A \oplus B\right)$$

$A + A = A$

$1 + A = 1$



Realization of Full Adder with two half Adders (*Picture is taken form: https://www.electrically4u.com/half-adder-and-full-adder/*)

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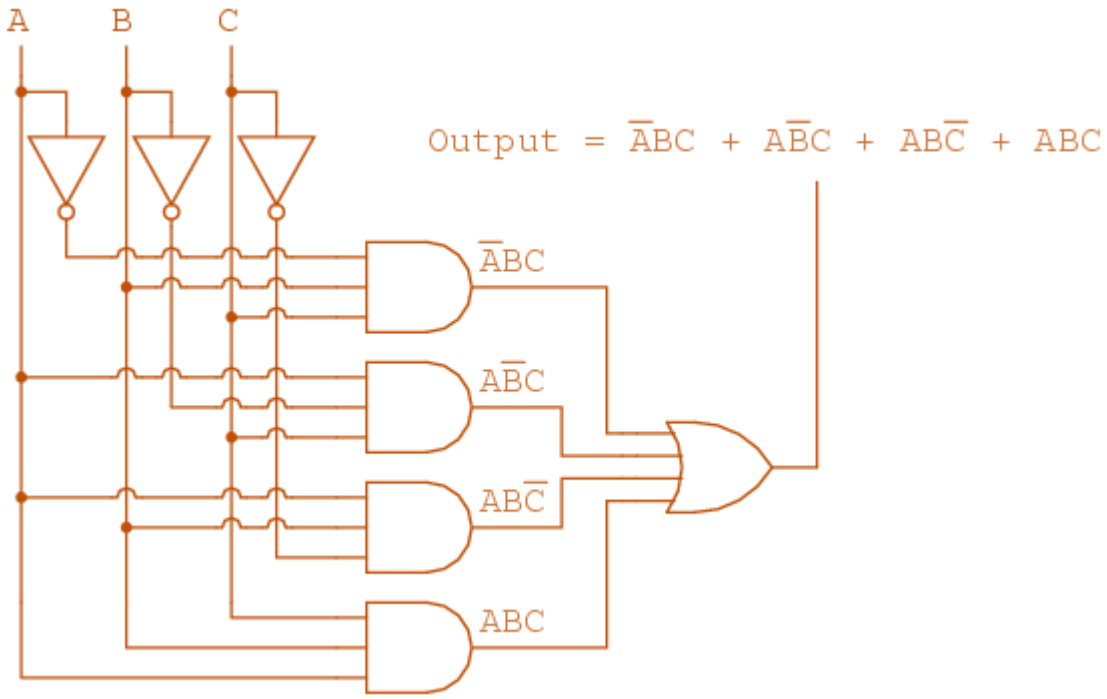
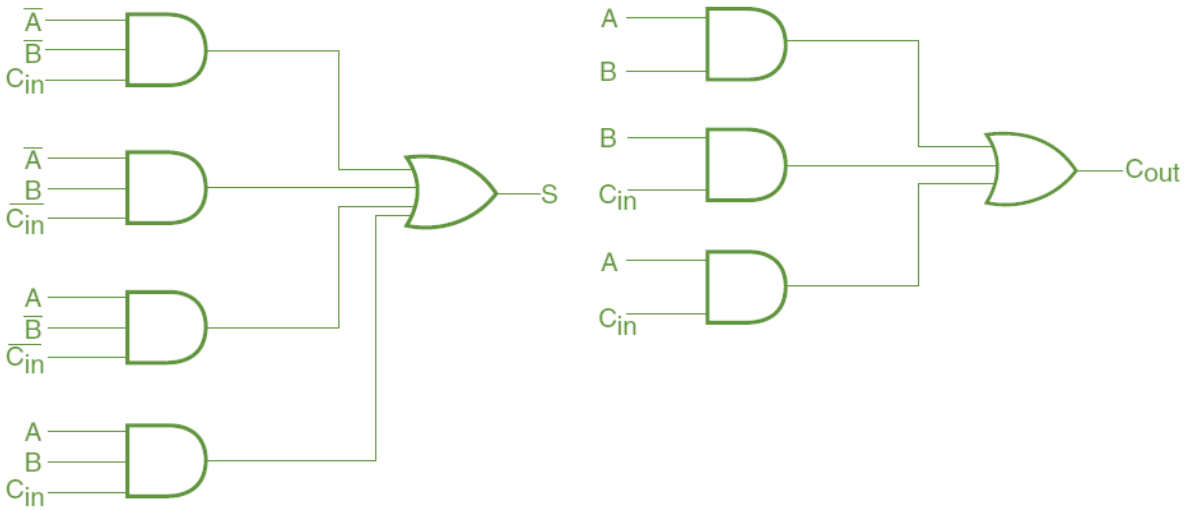


Circuit Diagram for SUM of Full Adder (Image source: *https://www.ibiblio.org/kuphaldt/electricCircuits/Digital/DIGI_7.html*)



Circuit Diagram for SUM and Carry of Full Adder

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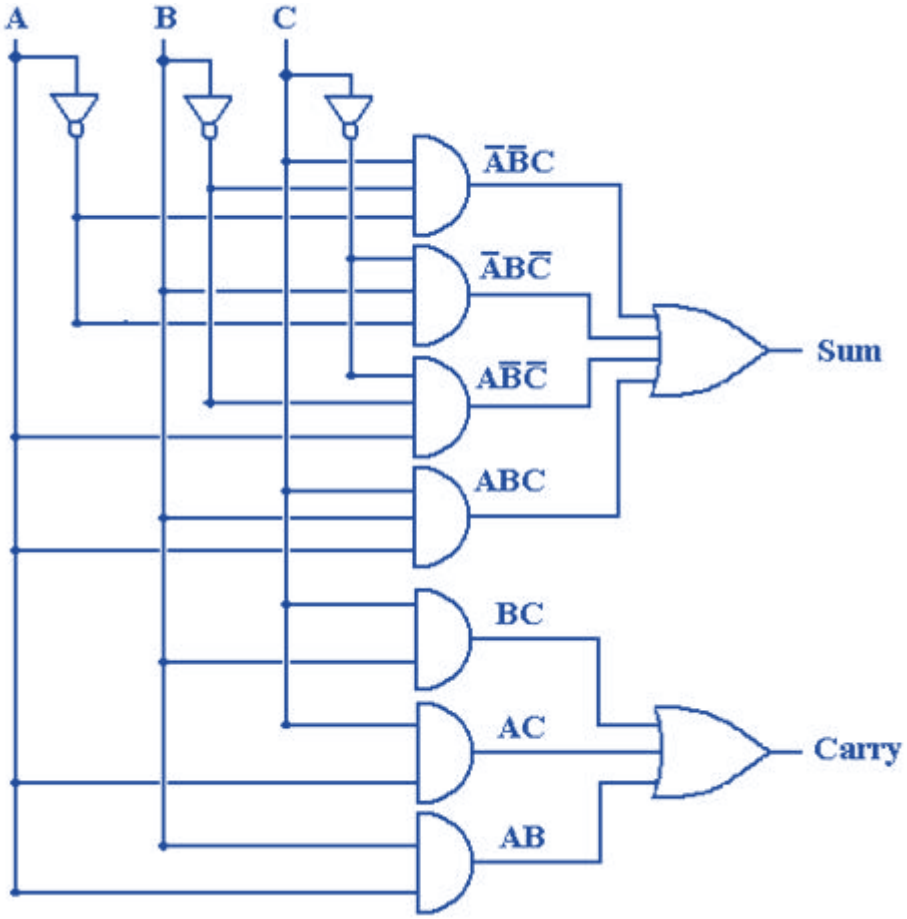

Circuit Diagram for SUM and Carry of Full Adder by Basic Gates

References:

(i) *Device Electronics for Integrated Circuits*, ***3rd Ed: R.S. Muller, T. I. Kamins, M. Chan, Published by WILEY (3rd Ed.).***
(ii) *Fundamental Principles of Electronics*, ***Author- B. Ghosh, Published by Books & Allied Pvt. Ltd. (2018 Ed.).***
(iii) *Digital Integrated Circuits A Design Perspective*- ***Author- J. M. Rabaey, A. Chandrakasan, B. Nicolic, Published by PEARSON. (2nd Ed.).***
(iv) *https://www.javatpoint.com/addition-and-subtraction-using-2s-complement-in-digital-electronics*
(v) *https://www.circuitstoday.com/half-adder*
(vi) *https://www.ques10.com/p/32990/explain-full-adder-circuit-using-pla-having-three-/*
(vii) *https://www.electronics-tutorial.net/combinational-logic-circuits/full-adder/*
(viii) *https://www.electrically4u.com/half-adder-and-full-adder/*
(ix) *https://www.ibiblio.org/kuphaldt/electricCircuits/Digital/DIGI_7.html*

(x) http://www.edwardbosworth.com/My5155_Slides/Chapter05/FullAdder.htm

Here images from different sources are taken only for the preparation of class notes.

Link to Audio visual Lectures (e-Lectures) and NPTEL lectures on this topic given by Distinguish Professors of Indian & Foreign Universities:

(1) https://nptel.ac.in/content/storage2/courses/117106114/Week9%20Slides/9.3Adder.pdf
(2) https://www.youtube.com/watch?v=KHgrJrcHr70
(3) https://nptel.ac.in/courses/108/105/108105113/
(4) https://nptel.ac.in/courses/117/105/117105080/