



College

Prof. Surajit Dhara

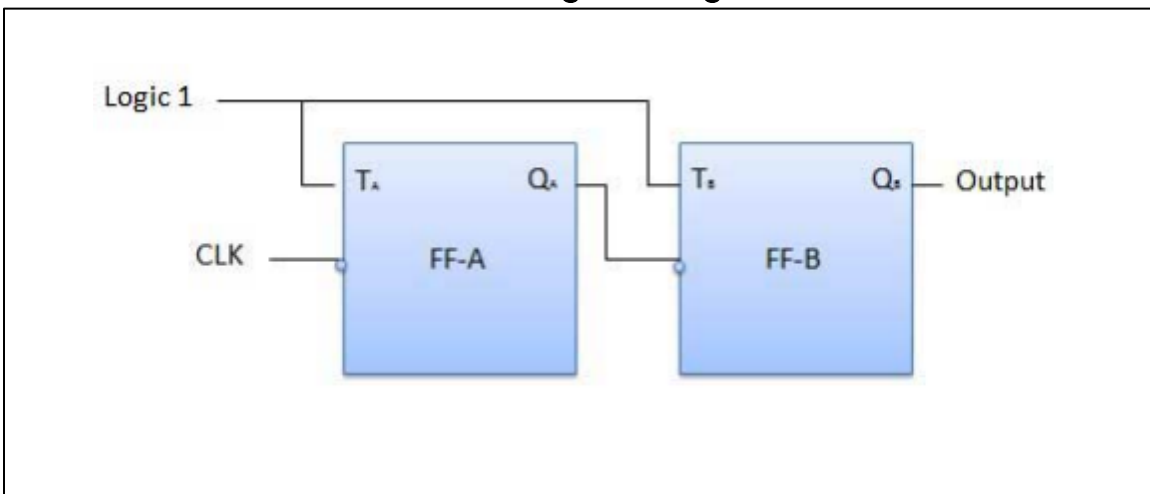
SACT,

Dept. Of Physics, Narajole Raj

C7T (Digital Systems and Applications) , Topic :- Counters

- ❖ **Counters:** Counter is a sequential circuit. A digital circuit which is used for a counting pulses is known counter. Counter is the widest application of flip-flops. It is a group of flip-flops with a clock signal applied. Counters are of two types
 - Asynchronous or ripple counters.
 - Synchronous counters.
- ❖ **Asynchronous or ripple counters:** The logic diagram of a 2-bit ripple up counter is shown in figure. The toggle T flip-flop are being used. But we can use the JK flip-flop also with J and K connected permanently to logic 1. External clock is applied to the clock input of flip-flop A and QA output is applied to the clock input of the next flip-flop i.e. FF-B.

Logical Diagram



| <u>Operation</u> | | |
|------------------|--|---|
| SL. No | Condition | Operation |
| 1. | Initially let both the FFs be in the reset state | $Q_B Q_A = 00$ initially |
| 2. | After 1st negative clock edge | <p>As soon as the first negative clock edge is applied, FF-A will toggle and Q_A will be equal to 1.</p> <p>Q_A is connected to clock input of FF-B. Since Q_A has changed from 0 to 1, it is treated as the positive clock edge by FF-B. There is no change in Q_B because FF-B is a negative edge triggered FF.</p> <p>$Q_B Q_A = 01$ after the first clock pulse.</p> |
| 3. | After 2nd negative clock edge | On the arrival of second negative clock edge, FF-A toggles again and $Q_A = 0$. The change in Q_A acts as a negative clock edge for FF-B. So |

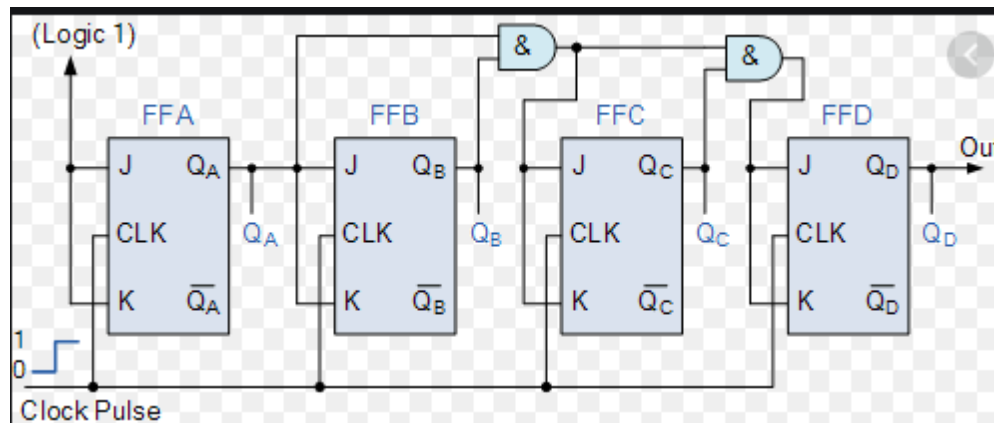
| | | |
|----|-------------------------------|---|
| | | <p>it will also toggle, and Q_B will be 1.</p> <p>$Q_B Q_A = 10$ after the second clock pulse.</p> |
| 4. | After 3rd negative clock edge | <p>On the arrival of 3rd negative clock edge, FF-A toggles again and Q_A become 1 from 0. Since this is a positive going change, FF-B does not respond to it and remains inactive. So Q_B does not change and continues to be equal to 1.</p> <p>$Q_B Q_A = 11$ after the third clock pulse.</p> |
| 5. | After 4th negative clock edge | <p>On the arrival of 4th negative clock edge, FF-A toggles again and Q_A becomes 1 from 0. This negative change in Q_A acts as clock pulse for FF-B. Hence it toggles to change QB from 1 to 0. $Q_B Q_A = 00$ after the fourth clock pulse</p> |

Truth Table

| Clock | Counter output | | State number | Deciimal Counter output |
|-----------|----------------|----------------|--------------|-------------------------|
| | Q _a | Q _b | | |
| Initially | 0 | 0 | — | 0 |
| 1st | 0 | 1 | 1 | 1 |
| 2nd | 1 | 0 | 2 | 2 |
| 3rd | 1 | 1 | 3 | 3 |
| 4th | 0 | 0 | 4 | 0 |

- ❖ **Synchronous counters** : If the "clock" pulses are applied to all the flip-flops in a counter simultaneously, then such a counter is called as synchronous counter.
- ❖ **4-bit Synchronous up counter** : The JA and KA inputs of FF-A are tied to logic 1. So FF-A will work as a toggle flip-flop. The JB and KB inputs are connected to QA.

Logical Diagram



Operation

| SL No. | Condition | Operation |
|--------|--|--|
| 1. | Initially let both the FFs be in the reset state | $Q_B Q_A = 00$ initially. |
| 2. | After 1st negative clock edge | <p>As soon as the first negative clock edge is applied, FF-A will toggle and Q_A will change from 0 to 1.</p> <p>But at the instant of application of negative clock edge, $Q_A, J_A = J_B = 0$. Hence FF-B will not change its state. So Q_B will remain 0.</p> <p>$Q_B Q_A = 01$ after the first</p> |

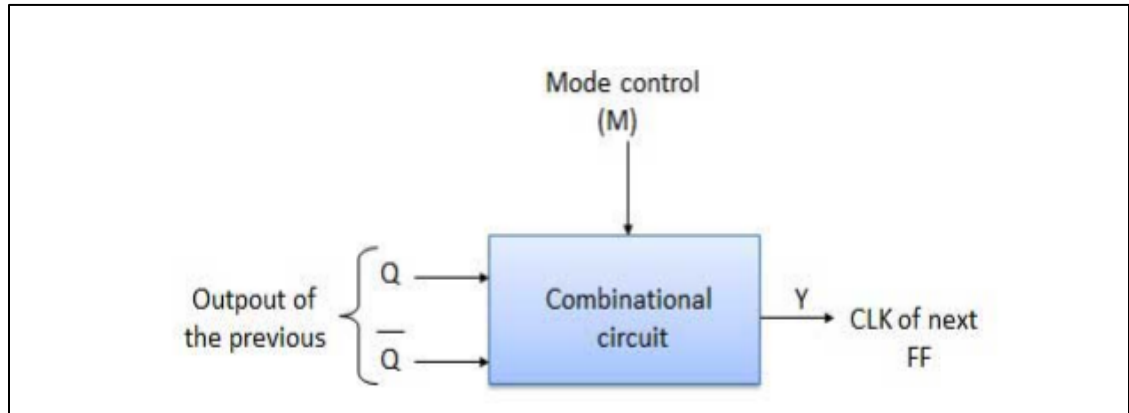
| | | |
|----|-------------------------------|---|
| | | clock pulse. |
| 3. | After 2nd negative clock edge | <p>On the arrival of second negative clock edge, FF-A toggles again and Q_A changes from 1 to 0.</p> <p>But at this instant Q_A was 1. So $J_B = K_B = 1$ and FF-B will toggle. Hence Q_B changes from 0 to 1.</p> <p>$Q_B Q_A = 10$ after the second clock pulse.</p> |
| 4. | After 3rd negative clock edge | <p>On application of the third falling clock edge, FF-A will toggle from 0 to 1 but there is no change of state for FF-B.</p> <p>$Q_B Q_A = 11$ after the third clock pulse.</p> |
| 5. | After 4th negative clock edge | <p>On application of the next clock pulse, Q_A will change from 1 to 0 as Q_B will also change from 1 to 0.</p> <p>$Q_B Q_A = 00$ after the fourth clock pulse.</p> |

- ❖ **Classification of counters** : Depending on the way in which the counting progresses, the synchronous or asynchronous counters are classified as follows –
 - Up counters
 - Down counters
 - Up/Down counters

- ❖ **UP/DOWN Counter** : Up counter and down counter is combined together to obtain an UP/DOWN counter. A mode control M input is also provided to select either up or down mode. A combinational circuit is required to be designed and used between each pair of flip-flop in order to achieve the up/down operation.
 - Type of up/down counters
 - UP/DOWN ripple counters
 - UP/DOWN synchronous counter
- ❖ **UP/DOWN Ripple Counters** : In the UP/DOWN ripple counter all the FFs operate in the toggle mode. So either T flip-flops or JK flip-flops are to be used. The LSB flip-flop receives clock directly. But the clock to every other FF is obtained from $Q = \bar{Q}$ output of the previous FF.
 - **UP counting mode $M = 0$** - The Q output of the preceding FF is connected to the clock of the next stage if up counting is to be achieved. For this mode, the mode select input M is at logic 0 $M = 0$.
 - **DOWN counting mode $M = 1$** - If $M = 1$, then the Q bar output of the preceding FF is connected to the next FF. This will operate the counter in the counting mode.
- ❖ **Example** : 3-bit binary up/down ripple counter.
 - 3-bit – hence three FFs are required.
 - UP/DOWN – So a mode control input is essential.
 - For a ripple up counter, the Q output of preceding FF is connected to the clock input of the next one.
 - For a ripple up counter, the Q output of preceding FF is connected to the clock input of the next one.
 - For a ripple down counter, the Q bar output of preceding FF is connected to the clock input of the next one.
 - Let the selection of Q and Q bar output of the preceding FF be controlled by the mode control input M such that, If $M = 0$, UP counting. So connect Q to CLK. If $M = 1$, DOWN counting. So connect

Q bar to CLK.

Block Diagram



Truth Table

| Inputs | | | Outputs |
|--------|---|----------------|---------|
| M | Q | \overline{Q} | Y |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Y = Q for up counter

Y = \overline{Q} for up counter

Operation

| SL No. | Condition | Operation |
|--------|--|---|
| 1. | Case 1 - With $M = 0$ Upcounting mode | <p>If $M = 0$ and $\bar{M} = 1$, then the AND gates 1 and 3 in fig. will be enabled whereas the AND gates 2 and 4 will be disabled.</p> <p>Hence QA gets connected to the clock input of FF-B and QB gets connected to the clock input of FF-C.</p> <p>These connections are same as those for the normal up counter. Thus with $M = 0$ the circuit work as an up counter.</p> |
| 2. | With $M = 1$ Downcounting mode | <p>If $M = 1$, then AND gates 2 and 4 in fig. are enabled whereas the AND gates 1 and 3 are disabled.</p> <p>Hence $\bar{Q}A$ gets connected to the clock input of FF-B and $\bar{Q}B$ gets connected to the clock input of FF-C.</p> <p>These connections will produce a down counter. Thus with $M = 1$ the circuit works as a down counter.</p> |

- ❖ **Modulus Counter MOD – N counter** : The 2-bit ripple counter is called as MOD-4 counter and 3-bit ripple counter is called as MOD-8 counter. So in general, an n-bit ripple counter is called as modulo-N counter. Where, MOD number = 2^n .
- ❖ **Type of modulus** :
 - 2-bit up or down MOD – 4

- 3-bit up or down MOD – 8
- 4-bit up or down MOD – 16

❖ **Application of counters :**

- Frequency counters
- Digital clock
- Time measurement
- A to D converter