Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

C10T (Analog Systems and Applications)

Topic – Amplifiers (Part – 7)

We have already discussed part 6 of this e-report.

Now let us continue part 7 of it.

Sub Topic – Conversion

Introduction:

Electronic signals can be of two types, *analog* and *digital*. A digital quantity will have a value that is specified as one of two possibilities such as 0 or 1, *Low* or *High*, *True* or *False*, and so on. In practice, the voltage representation a digital quantity such as a may actually have a value that is anywhere within specified ranges. For example, for a TTL logic, any voltage falling in the range $0 - 0.8$ V is given the digital value (or bit) 0, and any voltage in the range $2 - 5$ V is assigned the digital value (or bit) 1. The digital circuits respond accordingly to all voltage values within a given range.

Digital signals can be converted into an equivalent analog signal, and vice versa. There are two basic type of converters, *digital-to-analog converters* (DACs or D/As) and *analog-to-digital converters* (ADCs or A/Ds). Their purpose is fairly straightforward. In the case of DACs, they output an analog voltage that is a proportion of a reference voltage, the proportion based on the digital word applied. In the case of the ADC, a digital representation of the analog voltage that is applied to the ADCs input is outputted, the representation proportional to a reference voltage.

In both cases the digital word is almost always based on a binary weighted proportion. The digital input or output is arranged in words of varying widths, referred to as bits, typically anywhere from 6 bits to 24 bits. In a binary weighted system each bit is worth half of the bit to its left and twice the bit to its

Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

right. The greater the number of bits in the digital word, the finer the resolution. These bits are typically arranged in groups of four, called bytes, for convenience.

Digital-to-Analog Converter Architectures:

Basically, D/A conversion is the process of taking a value represented in digital code (such as straight binary or BCD) and converting it to a voltage or current which is proportional to the digital value. Fig. 1 shows the symbol for a typical 4-bit D/A converter.

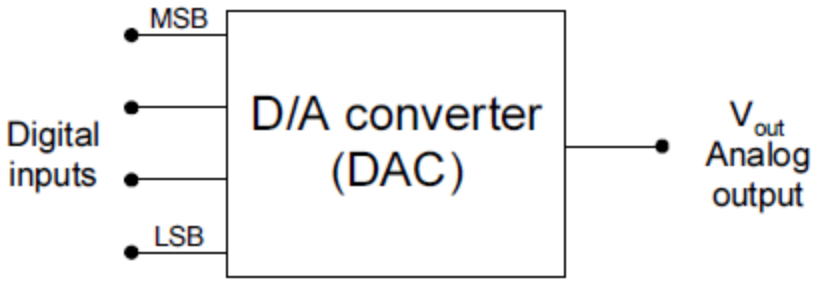

Fig. 1

The digital inputs D, C, B and A are usually derived from the output register of a digital system. The $2^4 = 16$ different binary numbers represented by these 4 bits for each input number, the D/A converter output voltage is a unique value. In fact, for this case, the analog output voltage V_{out} is equal in volts to the binary number.

In general, Analog output = $K \times$ digital input where K is the proportionality factor and it is constant value for a given DAC. The analog output can of course be a voltage or current. When it is a voltage, K will be in voltage units, and when the output is current, K will be in current units.

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There are several methods and circuits for producing the D/A operation. In this e-report we will examine two of those basic schemes to gain an insight into the ideas used.

Binary Weighted Circuit. Fig. 2 shows the basic circuit of 4-bit DAC. The inputs A, B, C and D are binary inputs which are assumed to have values of either 0 V or 5 V. Here A is the LSB (least significant bit) and D is the MSB (most significant bit). The operational amplifier is employed as a summing amplifier, which produces the weighted sum of these input voltages. The summing amplifier multiplies each input voltage by the ratio of the feedback resistor R_f to the corresponding input resistor R_i. In this circuit $R_f = 1$ kΩ and the input resistors range from 1 to 8 kΩ (in a multiplicative factor of 2). The D input has input resistor $R_D = 1$ kΩ, so the summing amplifier passes the voltage at D with no attenuation. The C input has $R_C = 2$ kΩ, so that it will be attenuated by $\frac{1}{2}$. Similarly, the B input will be attenuated by $\frac{1}{4}$ and the A input by $\frac{1}{8}$. The amplifier output can thus be expressed as

$$V_{out} = -R_f\left(\frac{V_D}{R_D} + \frac{V_c}{R_c} + \frac{V_B}{R_B} + \frac{V_A}{R_A}\right) = -\left(V_D + \frac{V_c}{2} + \frac{V_B}{4} + \frac{V_A}{8}\right)$$

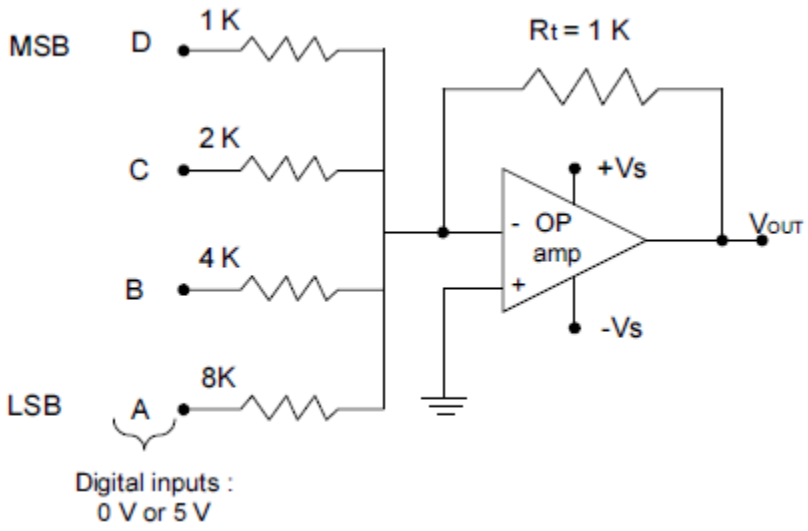

Fig. 2

Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
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The negative sign is present because the summing amplifier is an inverting amplifier, but it will not concern us here. Clearly, the summing amplifier output is an analog voltage which represents a weighted sum of the digital inputs. The output is evaluated for any input condition by setting the appropriate inputs to either 0 V or 5 V. For example, if the digital input is 1010_2, then $V_D = V_B = 5$ V and $V_C = V_A = 0$ V. Thus, using the previous equation, we obtain

$$V_{out} = -\left(5 + \frac{0}{2} + \frac{5}{4} + \frac{0}{8}\right) = -6.25 \text{ V}$$

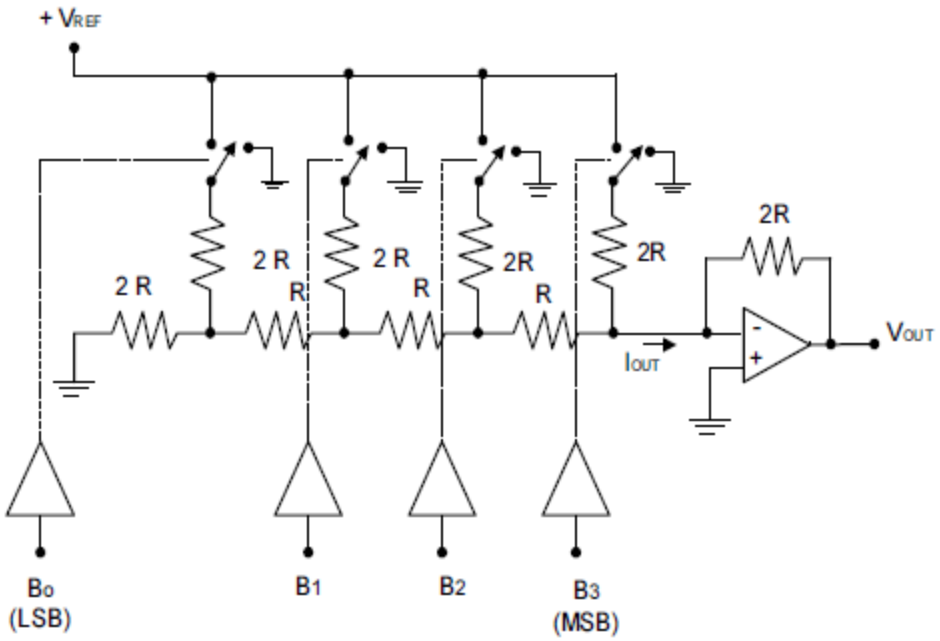

Fig. 3

***R* − 2*R* Ladder Circuit.** The DAC circuit we have looked at, has some practical limitations. The biggest problem is the large difference in resistor values between the LSB and MSB, especially in high-resolution DACs. One of the most widely used DAC circuits that uses resistance's fairly close in value is the $R - 2R$ ladder network. We discuss a 4-bit ladder network (Fig. 3). Here the resistance values span a range of only 2 to 1. It is important to note how the resistors are arranged, and only two different values are used, R and $2R$. The output current I_{out} depends on the positions of the four switches, and the binary

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Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

inputs B_3, B_2, B_1 and B_0 control the states of the switches. This current is allowed to flow through an Op-Amp current-to-voltage converter to develop V_{out}. It can be shown that the value of V_{out} is given by the expression $V_{out} = -\frac{V_{REF}}{8}B$, where B is the decimal value of the binary input, which can range from 0000_2 (i.e. 0) to 1111_2 (i.e. 15). In general, for a n-bit $R-2R$ ladder circuit (with R_f as the feedback resistor), the output voltage can be written as $V_{out} = -(\frac{R_f}{R_{Th}})(\frac{V_{REF}}{2^n})B$, where R_{Th} is the Thevenin equivalent resistor for the $R-2R$ ladder network.

Resolution and Accuracy of DACs:

Resolution. The percentage resolution of a DAC is dependent on the number of bits and it is expressed as a percentage of the full-scale output. To illustrate, let's assume that a DAC has a maximum full-scale output of 15 V (when the digital input is 1111_2). The step size is 1V, which gives a percentage resolution defined as, $\frac{\text{step size}}{\text{full-scale}} \times 100$. For the given example, % of resolution $= \frac{1}{15} \times 100 = 6.67\%$.

Accuracy. There are several ways of specifying accuracy. The most common method is called full-scale error. Full-scale error is the maximum deviation of the DAC's output from its expected (ideal) value, expressed as a percentage of full scale output. For example, assume that the DAC has an accuracy of ± 0.01% FS. If this converter has a full-scale output of 9.375 V, (say) this percentage converts to ± 0.01% × 9.375 V = ± 0.9375 mV This means that the output of this DAC can, at any time, be off by as much as 0.9375 mV from its expected value.

Analog-to-Digital Converter Architectures:

An analog-to-digital converter takes an analog input voltage and after a certain amount of time produces a digital output code which represents the analog input. The A/D conversion process is generally more complex and time-

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Department of Physics,
Narajole Raj College, Narajole.

consuming than the D/A process. The techniques that are used to provide and insight into what factors determine an ADCs performance.

Several important types of ADC utilize a DAC as part of their circuitry. Fig. 4 is a general block diagram for this class of ADC. The timing for the operation is provided by the input clock signal. The control unit contains the logic circuitry for generating the proper sequence of operations. The Start Command initiates the conversion process. The op-amp compactor has two analog inputs and a digital output that switches states, depending on which analog input is greater.

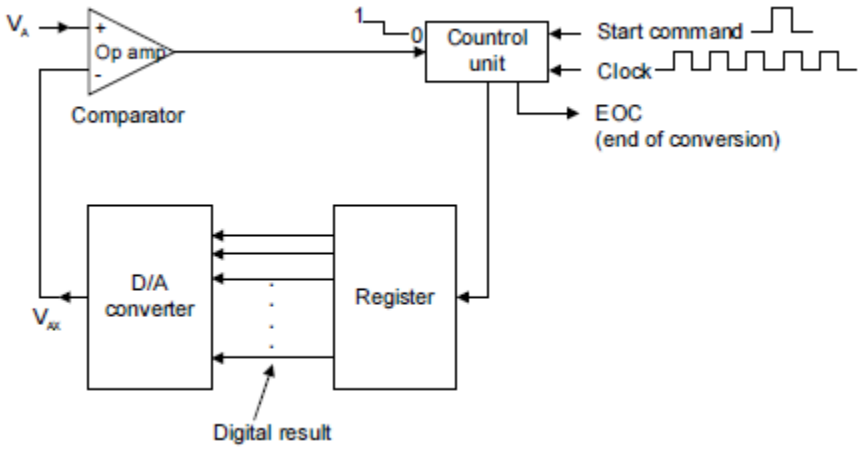

Fig. 4

The basic operation of ADCs of this type consists of the following steps:

1. The Start Command pulse initiates the operation.

2. At a rate determined by the clock, the control unit continually modifies the binary number that is stored in the register.

3. The binary number in the register is converted to an analog voltage V_{AX}, by the DAC.

4. The comparator compares V_{AX} with the analog input V_A. As long as $V_{AX} < V_A$, the comparator output stays *High*. When V_{AX} exceeds V_A by at least an amount V_T (the threshold voltage), the comparator output goes *Low* and stops the

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Narajole Raj College, Narajole.

process of modifying the register number. At this point, V_{AX} is a close approximation to V_A. The digital number in the register, which is the digital equivalent of V_{AX}, is also the approximate digital equivalent of V_A within the resolution and accuracy of the system.

5. The control logic activates the end-of-conversion signal, EOC, when the conversion is complete.

Successive Approximation ADC. The successive approximation ADC has been the mainstay of data acquisition for many years. Recent design improvements have extended the sampling frequency of these ADCs into the MHz region.

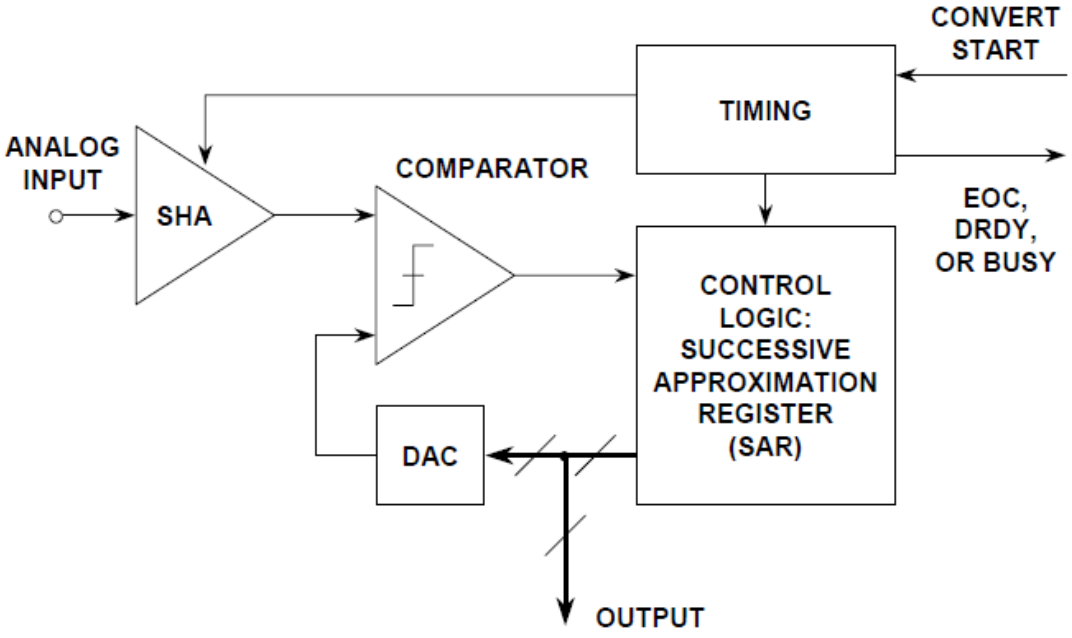

Fig. 5

The basic successive approximation ADC is shown in Fig. 5. It performs conversions on command. On the assertion of the Convert Start command, the sample-and-hold (SHA) is placed in the hold mode, and all the bits of the successive approximation register (SAR) are reset to 0 except the MSB which is set to 1. The SAR output drives the internal DAC. If the DAC output is greater

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than the analog input, this bit in the SAR is reset, otherwise it is left set. The next most significant bit is then set to 1. If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The process is repeated with each bit in turn. When all the bits have been set, tested and reset or not as appropriate, the contents of the SAR correspond to the value of the analog input, and the conversion is complete. These bit "tests" can form the basis of a serial output version SAR-based ADC.

Reference(s):

Circuit Design Handbook, Hank Zumbahlen, Newnes-Elsevier

Digital Systems and Computer Organization, School of Science and Technology, Bangladesh Open University

(All the figures have been collected from the above mentioned references)