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IC 555 Multivibrator Circuits

❖ Multivibrators :

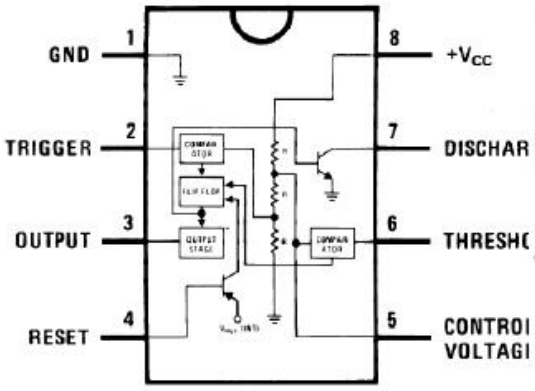
Individual **Sequential Logic** circuits can be used to build more complex circuits such as Counters, Shift Registers, Latches or Memories etc, but for these types of circuits to operate in a "Sequential" way, they require the addition of a clock pulse or timing signal to cause them to change their state. **Clock pulses** are generally square shaped waves that are produced by a single pulse generator circuit such as a **Multivibrator** which oscillates between a "HIGH" and a "LOW" state and generally has an even 50% duty cycle, that is it has a 50% "ON" time and a 50% "OFF" time. Sequential logic circuits that use the clock signal for synchronization may also change their state on either the rising or falling edge, or both of the actual clock signal. There are basically three types of pulse generation circuits depending on the number of stable states,

- Astable - has **NO** stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed frequency.
- Monostable - has only **ONE** stable state and if triggered externally, it returns back to its first stable state.
- Bistable - has **TWO** stable states that produces a single pulse either positive or negative in value.

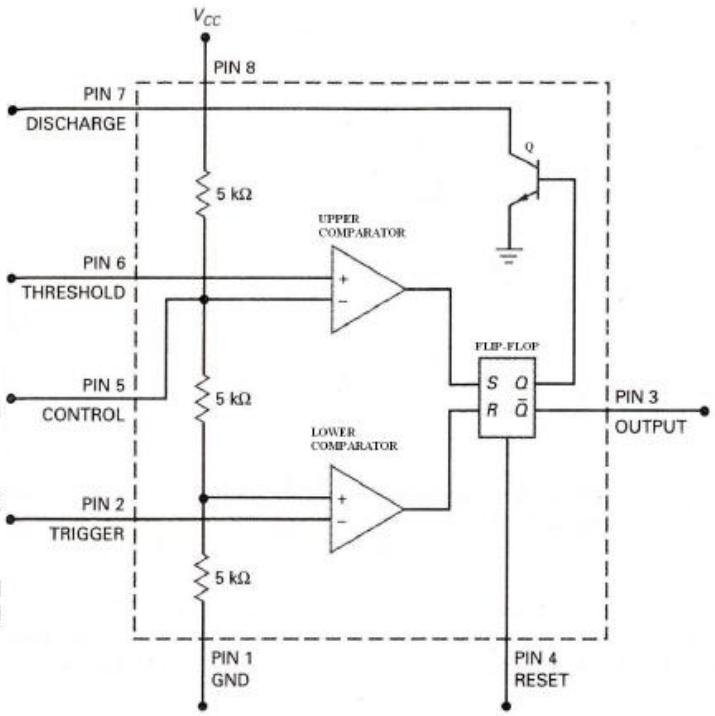
❖ IC 555 TIMER :

The 555 timer IC was first introduced around 1971 by the Signetics Corporation as the SE555/NE555 and was called "**The IC Time Machine**" and was also the very first and only commercial timer IC available. It provided circuit designers with a relatively cheap, stable, and user-friendly integrated circuit for timer and multivibrator applications. These ICs come in two packages, either the round metal-can called the 'T' package or the more familiar 8-pin DIP 'V' package as

shown in figure below. The IC comprises of 23 transistors, 2 diodes and 16 resistors with built-in compensation for component tolerance and temperature drift.



IC 555 in 8-pin DIP package



Functional block diagram of IC 555

- The pin connections are as follows:
  1. Ground
  2. Trigger input.
  3. Output.
  4. Reset input.
  5. Control voltage.
  6. Threshold input
  7. Discharge.
  8. + V_{CC}. +5 to +15 volts in normal use.

Pin1: Ground. All voltages are measured with respect to this terminal.

Pin2: Trigger. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. When a negative going pulse of amplitude greater than 1/3 V_{CC} is applied to this pin, the output of the timer high. The output remains high as long as the trigger terminal is held at a low voltage.

Pin3: Output. The output of the timer is measured here with respect to ground. There are two ways by which a load can be connected to the output terminal: either between pin 3 and ground or between pin3 and supply voltage + V_{CC}. When the output is low the load current flows through the load connected between pin3 and + V_{CC} into the output terminal and is called sink current. The current through the grounded load is zero when the output is low. For this reason the load connected between pin 3 and + V_{CC} is called the *normally on load* (we will use this for our circuit) and that connected between pin 3 and ground is called *normally off-load*. On the other hand, when the output is high the current through the load connected between pin 3 and + V_{CC} is zero. The output terminal supplies current to the normally off load. This current is called source current. The maximum value of sink or source current is 200mA.

Pin4: *Reset*. The 555 timer can be reset (*disabled*) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to + V_{CC} to avoid any possibility of false triggering.

Pin5: *Control Voltage*. An external voltage applied to this terminal changes the threshold as well as trigger voltage. Thus by imposing a voltage on this pin or by connecting a *pot* between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a 0.01μF Capacitor to prevent any noise problems.

Pin6: *Threshold*. When the voltage at this pin is greater than or equal to the threshold voltage 2/3 *VCC*, the output of the timer low.

Pin7: *Discharge*. This pin is connected internally to the collector of transistor Q. When the output is high Q is OFF and acts as an open circuit to external capacitor C connected across it. On the other hand, when the output is low, Q is saturated and acts as a short circuit, shorting out the external capacitor C to ground.

Pin8: + V_{CC}. The supply voltage of +5V to + 18V is applied to this pin with respect to Ground.

- **OPERATION:** The functional block diagram shows that the device consists of two comparators, three resistors and a flip-flop. A comparator is an OPAMP that compares an input voltage and indicates whether an input is higher or lower than a reference voltage by swinging into saturation in both the direction. The operation

of the 555 timer revolves around the three resistors that form a voltage divider across the power supply to develop the reference voltage, and the two comparators connected to this voltage divider. The IC is quiescent so long as the trigger input (pin 2) remains at $+V_{CC}$ and the threshold input (pin 6) is at ground. Assume the reset input (pin 4) is also at $+V_{CC}$ and therefore inactive, and that the control voltage input (pin 5) is unconnected.

The three resistors in the voltage divider all have the same value (5K in the bipolar version of this IC and hence the name 555), so the trigger and threshold comparator reference voltages are 1/3 and 2/3 of the supply voltage, respectively. The control voltage input at pin 5 can directly affect this relationship, although most of the time this pin is unused. The internal flip-flop changes state when the trigger input at pin 2 is pulled down below $+V_{CC}$ /3. When this occurs, the output (pin 3) changes state to $+V_{CC}$ and the discharge transistor (pin 7) is turned off. The trigger input can now return to $+V_{CC}$; it will not affect the state of the IC.

However, if the threshold input (pin 6) is now raised above $+(2/3)\ V_{CC}$, the output will return to ground and the discharge transistor will be turned on again. When the threshold input returns to ground, the IC will remain in this state, which was the original state when we started this analysis. The easiest way to allow the threshold voltage (pin 6) to gradually rise to $+(2/3)\ V_{CC}$ is to connect it externally to a capacitor being allowed to charge through a resistor. In this way we can adjust the R and C values for almost any time interval we might want.

- **IC 555 Timer as Multivibrator :**

The 555 can operate in either mono/bi-stable or astable mode, depending on the connections to and the arrangement of the external components. Thus, it can eitherproduce a single pulse when triggered, or it can produce a continuous pulse train as longas it remains powered.

- **Astable Multivibrator:** These circuits are not stable in any state and switch outputs after predetermined time periods. The result of this is that the output is a continuous square/rectangular wave with the properties depending on values of external resistors and capacitors. Thus, while designing these circuits following parameters need to be determined:

1. Frequency (or the time period) of the wave.
2. The duty cycle of the wave.

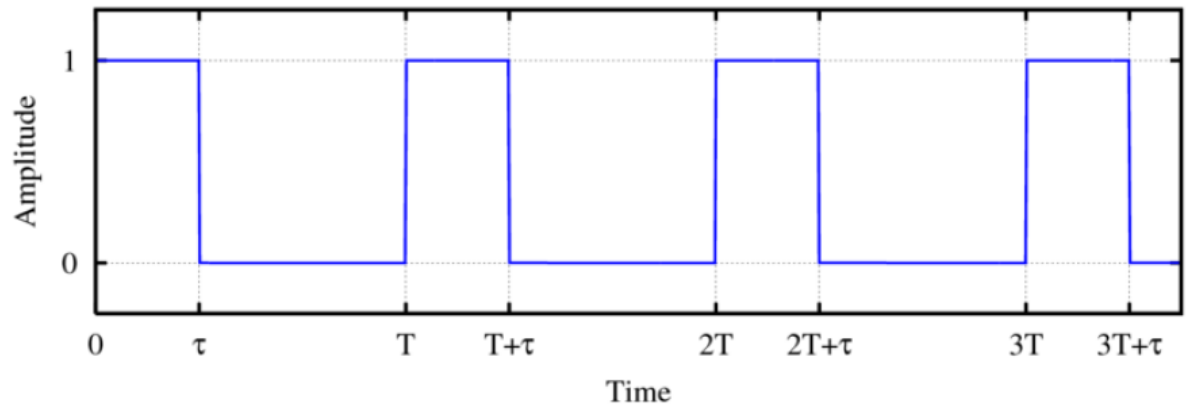


Figure 1: A rectangular waveform

Referring to the above figure of a rectangular waveform, the time period of the pulse is defined as T and duration of the pulse (ON time) is τ. Duty cycle can be defined as the On time/Period that is, τ/T in the above figure. Obviously, a duty cycle of 50% will yield a square wave.

The key external component of the **astable timer** is the *capacitor*. An astable multivibrator can be designed as shown in the circuit diagram (with typical component values) using IC 555, for a duty cycle of more than 50%. The corresponding voltage across the capacitor and voltage at output is also shown. The astable function is achieved by charging/discharging a capacitor through resistors connected, respectively, either to V_{CC} or GND. Switching between the charging and discharging modes is handled by resistor divider R_1-R_3, two Comparators, and an RS Flip-Flop in IC 555. The upper or lower comparator simply generates a positive pulse if $+V_{CC}$ goes above 2/3 V_{CC} or below
1/3 V_{CC}. And these positive pulses either SET or RESET the Q output.

The time for charging C from 1/3 to 2/3 Vcc, i.e, **ON Time = 0.693 (R_A + R_B). C**
The time for discharging C from 2/3 to 1/3 Vcc, i.e. **OFF Time = 0.693 R_B. C**
To get the total oscillation period, just add the two:

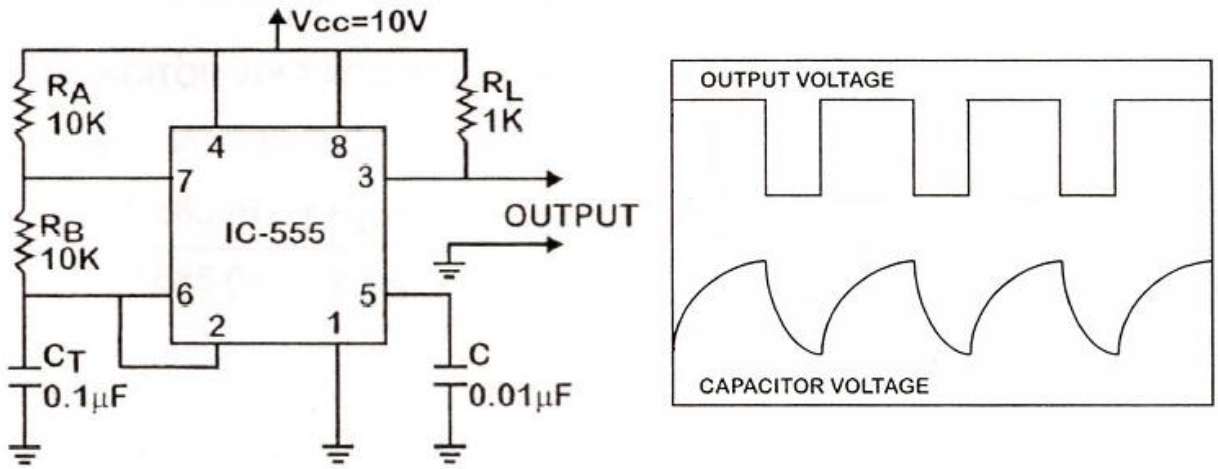
$$\textbf{Tosc} = 0.693(R_A+R_B)C + 0.693(R_B)C = 0.693\,(R_A + 2R_B)C$$

Thus,

$$\textbf{fosc} = 1/\,\textbf{Tosc} = 1.44/(\,R_A + 2R_B).C$$

$$\textbf{Duty cycle} = R_A+R_B/\,R_A + 2R_B$$

Circuit Diagram:



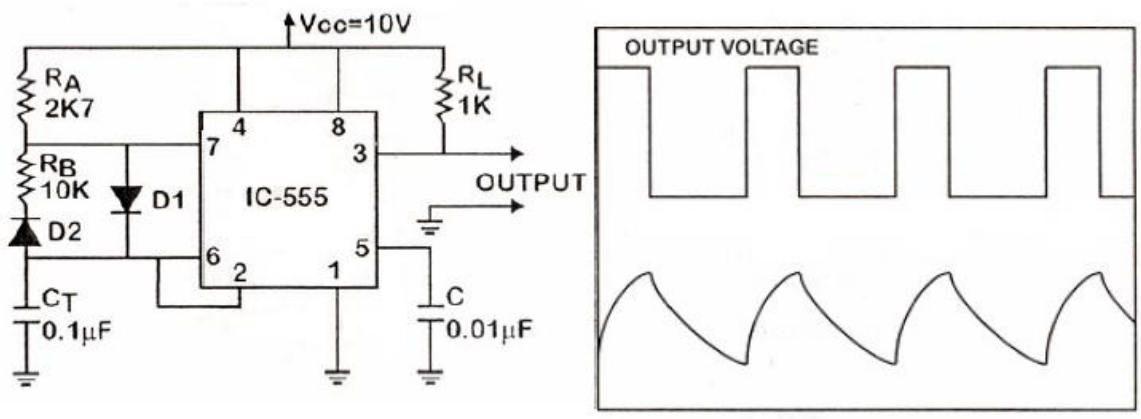
Astable multivibrator with duty cycle less than 50%:

Generally astable mode of IC 555 is used to obtain the duty cycle between 50 to 100%. But for a duty cycle less than 50%, the circuit can be modified as per the circuit diagram. Here a diode D1 is connected between the discharge and threshold terminals (as also across R_B). Thus the capacitor now charges only through R_A (since R_B is shorted by diode conduction during charging) and discharges through RB. Another optional diode D2 is also connected in series with R_B in reverse direction for better shorting of RB. Therefore, the frequency of oscillation and duty cycle are

$$\mathbf{fosc = 1/ Tosc = 1.44/(R_A + R_B).C}$$

$$\mathbf{Duty\ Cycle = R_A/ (R_A + R_B)}$$

Circuit Diagram:



Astable multivibrator with duty cycle variable from 0 to 100%:

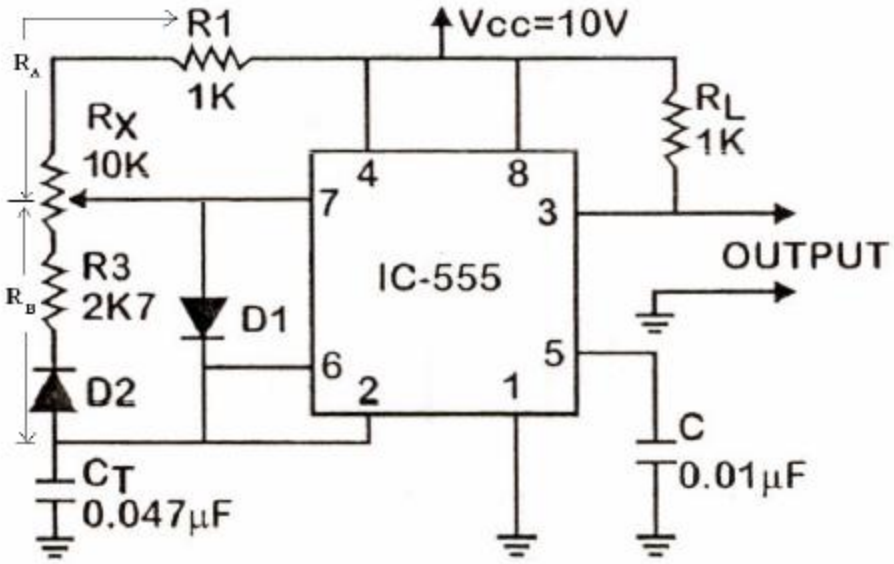
In some applications, it is needed to vary the duty cycle from about 0 to 100%. In that case the circuit is designed as shown in the circuit diagram. Here a potentiometer, R_X, is used so that $R_A = R_1+R_2$, $R_B = R_X-R_2+R_3$. A diode is now connected across a variable RB. Thus a variable duty cycle is achieved. Therefore, the frequency of oscillation and duty cycle can be derived as follows.

$$\mathbf{fosc = 1/ Tosc = 1.44/(R_A + R_B).C = 1.44/(R_1 + R_X + R_3).C}$$

$$\mathbf{Min.\ Duty\ Cycle = R_1/(R_1 + R_X + R_3)}$$

$$\mathbf{Max.\ Duty\ Cycle = (R_1 + R_X)/(R_1 + R_X + R_3)}$$

Circuit Diagram:

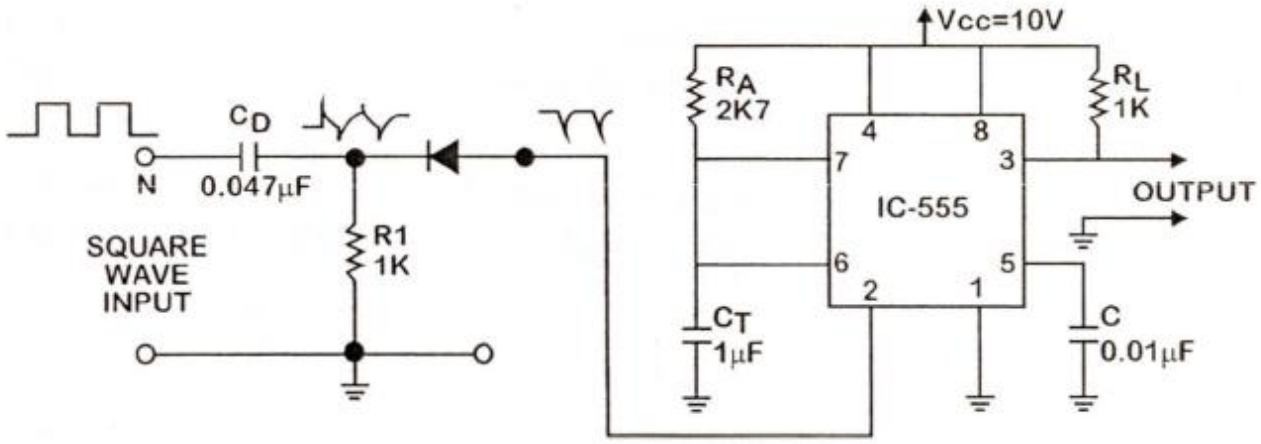


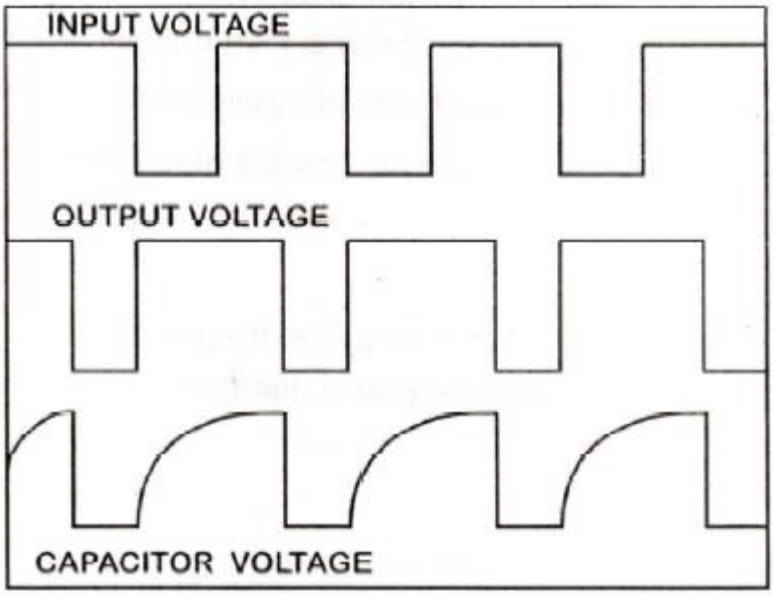
Monostable multivibrator: Monostable multivibrator often called a *one shot* multivibrator is a pulse generating circuit in which the duration of this pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby state, the output of the circuit is approximately zero or a logic-low level. When external trigger pulse is applied (See circuit diagram) output is forced to go high (» V_{CC}). The time for which output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (*output low*) hence the name *monostable*.

Initially when the circuit is in the stable state i.e, when the output is low, transistor Q in IC 555 is ON and the capacitor C is shorted out to ground. Upon the application of a negative trigger pulse to pin 2, transistor Q is turned OFF, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards $+V_{CC}$ through R. When the voltage across the capacitor equals 2/3 V_{CC}, the upper comparator's (see schematics of IC 555) output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time the output of the flip-flop turns transistor Q ON and hence the capacitor C rapidly discharges through the transistor. The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats. The pulse width of the trigger input must be smaller than the expected pulse width of the output

waveform. Also the trigger pulse must be a negative going input signal with amplitude larger than 1/3 V_{CC} (Why?). The pulse width can be calculated as (How?): **T= 1.1 R.C.** Once triggered, the circuit's output will remain in the high state until the set time, T, elapses. The output will not change its state even if an input trigger is applied again during this time interval. The circuit can be reset during the timing cycle by applying negative pulse to the reset terminal. The output will remain in the low state until a trigger is again applied. The circuit is designed as shown in the circuit diagram, the left part of which shows how to generate negative a trigger pulse from a square wave signal.

Circuit Diagram:




INPUT VOLTAGE
OUTPUT VOLTAGE
CAPACITOR VOLTAGE