Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

C10T (Analog Systems and Apllications)

Topic - Field Effect Transistors

Introduction:

In a field effect transistor (FET), the output characteristics are controlled by *input voltage* (i.e., an *electric field*) and not by *input current* like a bipolar junction transistor (BJT). This is probably the biggest difference between a BJT and a FET.

The ordinary transistor or BJT has two principal disadvantages. First, it has relatively low input impedance because of forward biased emitter junction. Secondly, it has considerable noise level. Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few megaohms (MΩ). The field effect transistor (FET) has, by virtue of its construction and biasing, large input impedance which may be more than 100 MΩ. The FET is generally much less noisy than the ordinary or bipolar transistor.

There are two basic types of field effect transistors:

(i) Junction field effect transistor (JFET)

(ii) Metal oxide semiconductor field effect transistor (MOSFET)

In this e-report, only JFETs have been discussed.

Junction Field Effect Transistor (JFET):

A JFET is a three terminal semiconductor device in which current conduction is by *one type of carrier* i.e., electrons or holes.

It is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The JFET has high input impedance and low noise level.

Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

Constructional details. A JFET consists of a p-type or n-type silicon bar containing two p-n junctions at the sides as shown in Fig. 1. The bar forms the conducting channel for the charge carriers. If the bar is of n-type, it is called *n-channel JFET* as shown in Fig. 1(i) and if the bar is of p-type, it is called a *p-channel JFET* as shown in Fig. 1(ii). The two p-n junctions forming diodes are connected internally and a common terminal called *gate* is taken out. Other terminals are *source* and *drain*, taken out from the bar as shown. Thus a JFET has essentially three terminals viz., gate (G), source (S) and drain (D).

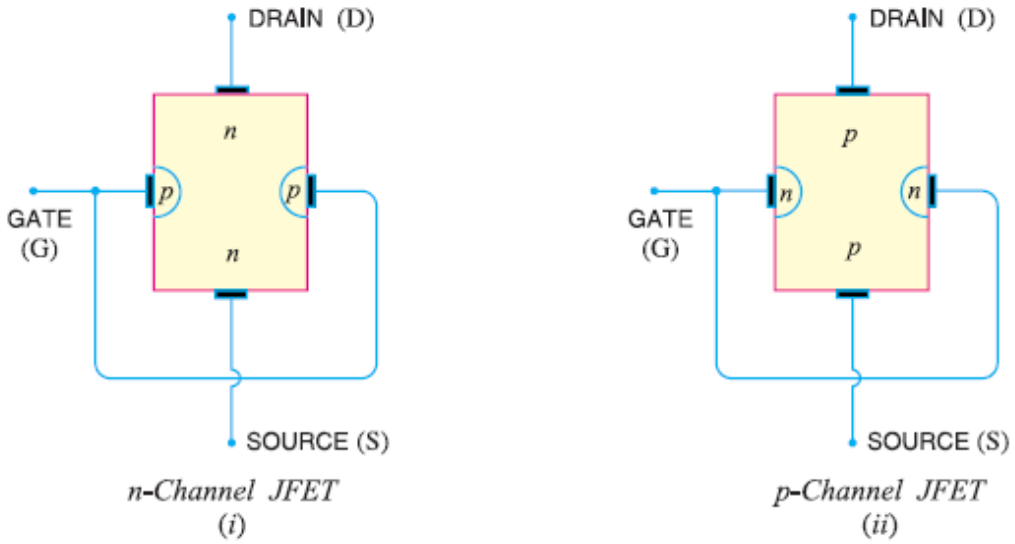

Fig. 1

Working Principle of a JFET:

Principle. The two p-n junctions at the sides form two depletion layers. The current conduction by charge carriers (i.e. free electrons in this case) is through the channel between the two depletion layers and out of the drain. The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS}. The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}. In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS}.

Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

Working Methodology. The working methodology of JFET is as under:

(i) When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero [Fig. 2(*i*)], the two p-n junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

(ii) When a reverse voltage V_{GS} is applied between the gate and source [Fig. 2(*ii*)], the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from source to drain is decreased.

On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.

It is clear from the above discussion that current from source to drain can be controlled by the application of potential (i.e. electric field) on the gate. For this reason, the device is called *field effect transistor*. It may be noted that a p-channel JFET operates in the same manner as an n-channel JFET except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

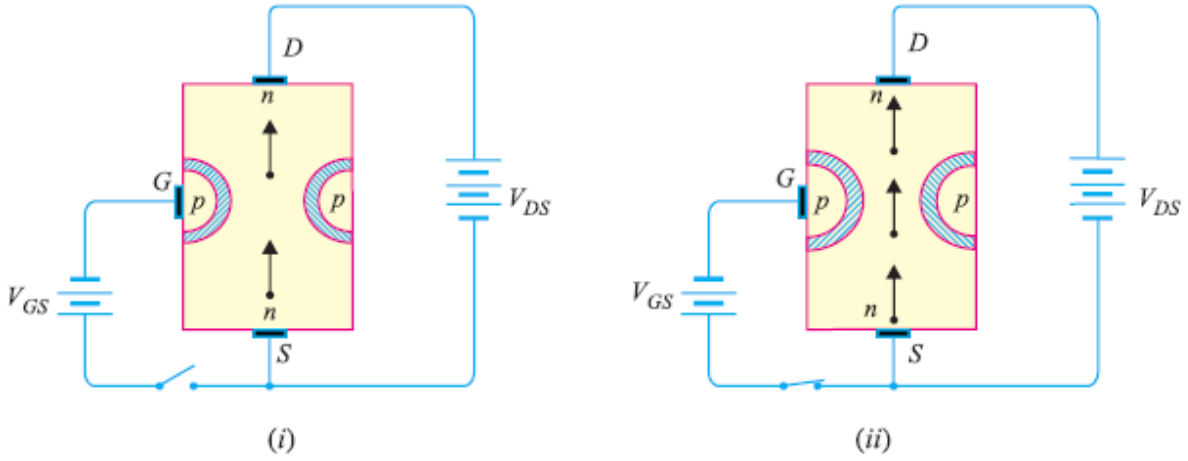

Fig. 2

PAPER: C10T (Analog Systems and Applications)
TOPIC(s): Field Effect Transistors

Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

Schematic Symbol of a JFET:

Fig. 3 shows the schematic symbol of JFET. The vertical line in the symbol may be thought as channel and source (S) and drain (D) connected to this line. If the channel is n-type, the arrow on the gate points towards the channel as shown in Fig. 3(i). However, for p-type channel, the arrow on the gate points from channel to gate [as shown in Fig. 3(ii)].

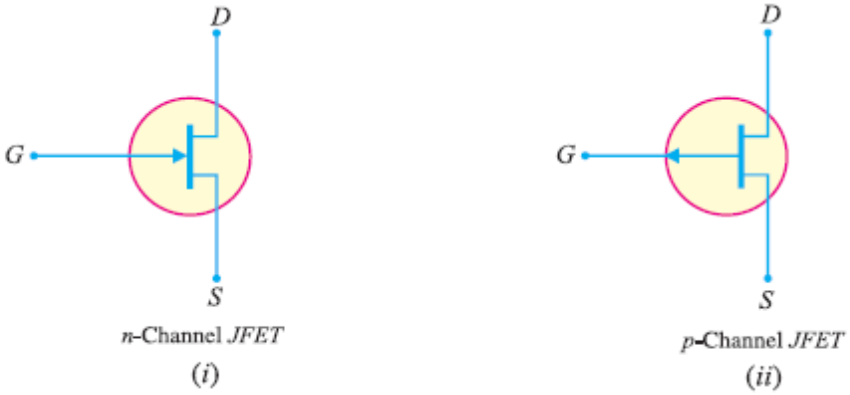

Fig. 3

Output Characteristics of a JFET:

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a JFET (n-channel) at constant gate source voltage (V_{GS}) is known as *output characteristics* of JFET. Fig. 4 shows the circuit for determining the output characteristics of JFET. Keeping V_{GS} fixed at some value, say 1 V, the drain source voltage is changed in steps. Corresponding to each value of V_{DS}, the drain current I_D is noted.

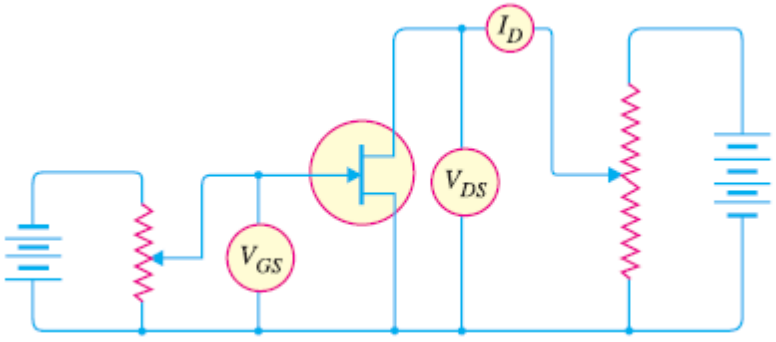

Fig. 4

Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

A plot of these values gives the output characteristic of JFET at $V_{GS} = 1$ V. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. 5 shows a family of output characteristics.

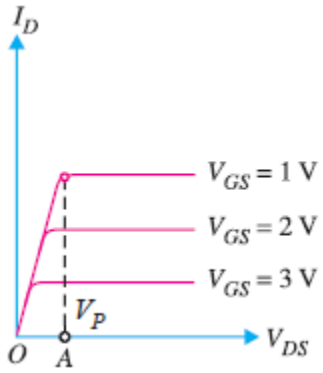

Fig. 5

The following points may be noted from the characteristics:

(i) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as *pinch-off voltage* V_P. Thus in Fig. 5, the point A is the pinch off voltage V_P.

(ii) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch off voltage. Consequently, drain current remains constant.

Salient Features of a JFET:

The following are some salient features of JFET:

(i) A JFET is a three-terminal voltage-controlled semiconductor device i.e. input voltage controls the output characteristics of JFET.

(ii) The JFET is always operated with gate-source p-n junction reverse biased.

(iii) In a JFET, the gate current is zero i.e. $I_G = 0$ A.

(iv) Since there is no gate current, $I_D = I_S$.

Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

(v) The JFET must be operated between V_{GS} and $V_{GS(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

(vi) Because the two gates are at the same potential, both depletion layers widen or narrow down by an equal amount.

(vii) The JFET is not subjected to thermal runaway when the temperature of the device increases.

(viii) The drain current I_D is controlled by changing the channel width.

Transfer Characteristics of a JFET, Shockley's Equation:

The relation between I_{DSS} and V_P is shown in Fig. 6. We note that gate-source cut off voltage [i.e. $V_{GS(off)}$] on the *transfer characteristics* is equal to pinch off voltage V_P on the drain characteristics i.e.

$$V_P = |V_{GS(off)}|$$

For example, if a JFET has $V_{GS(off)} = -4$ V, then $V_P = 4$ V.

The transfer characteristics of JFET shown in left side of Fig. 6 is part of a parabola. A rather complex mathematical analysis done by Shockley yields the following expression for drain current, known as *Shockley's Equation*:

$$I_D = I_{DSS} \times \left\{1 - \frac{V_{GS}}{V_{GS(off)}}\right\}^2$$

where I_D is the drain current at a given V_{GS}.

I_{DSS} = shorted–gate drain current

V_{GS} = gate–source voltage

$V_{GS(off)}$ = gate–source cut off voltage

Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

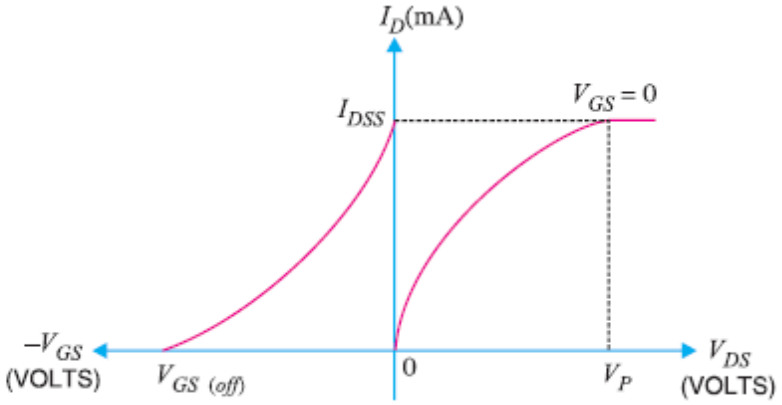

Fig. 6

Some Important Terms:

In the analysis of a JFET circuit, the following important terms are often used:

1. Shorted-gate drain current (I_{DSS}). It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage. It is sometimes called *zero-bias current*.

2. Pinch off Voltage (V_P). It is the minimum drain-source voltage at which the drain current essentially becomes constant.

3. Gate-source cut off voltage ($V_{GS(off)}$). It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.

Advantages of JFET:

A JFET is a voltage controlled, constant current device (similar to a vacuum pentode) in which variations in input voltage control the output current. It combines the many advantages of both bipolar transistor and vacuum pentode. Some of the advantages of a JFET are:

(i) It has very high input impedance (of the order of 100 MΩ). This permits high degree of isolation between the input and output circuits.

Dr. Avradip Pradhan,
Assistant Professor,
Department of Physics,
Narajole Raj College, Narajole.

(ii) The operation of a JFET depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a JFET.

(iii) A JFET has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

(iv) A JFET has a very high power gain. This eliminates the necessity of using driver stages.

(v) A JFET has a smaller size, longer life and high efficiency.

Reference:

Principles of Electronics, V.K. Mehta & Rohit Mehta, S. Chand & Company

(All the figures have been collected from the above mentioned reference)